ABSTRACT

[0060] An on-chip reduced complexity modulation noise estimation mechanism for performing nonlinear signal processing to analyze modulation noise to determine whether a semiconductor device under test complies with the performance criteria set by specifications or a standard corresponding thereto. When used in a two-point transmitter modulation architecture, the mechanism relies on the fact that the noise statistics at the output of the transmitter can be determined by observing the phase error output of the phase detector within the phase locked loop. In the digital embodiment of the mechanism, the phase error signal is compared to a configurable threshold value to generate an exception event. If the number of exception events exceeds a configurable max_fail value after comparisons of a configurable number of phase error samples, the test fails. A pass/fail signal is output reflecting the result of the test. The test comprises a configurable number of test samples to permit flexibility in the tradeoff between the time required to complete the test versus the statistical reliability of the test result, i.e. the probability of it correctly determining whether the tested device complies with target specifications.